

## Detailed Description Text - DETX (26).

The current design of the electronic circuitry of FIG. 6 is intended to have the application processing task 108 be replaceable with other types of processing depending upon the application or type of symbol reader the design is to be used in the application processing task 108 will set the priorities of the other tasks (tasks 160, 104, 112, and 108). Since the application processing task 108 has the capability of setting the task priorities (Step 816, FIG. 8), it also has the capability of altering the priorities according to need. Thus, for example, if a symbology is selected to be read that is so complex as to require sufficient decoding processing time to bottleneck system throughput, then the application processing task can dynamically change the priority (Step 816, FIG. 8) of the label decode task 104 to be the highest priority task for execution, and this task would execute as long as inputs existed for it to decode. Further, if one application using this design requires more (or less) tasks than the current application, then the application processing task 108 can create the number of tasks needed. For example, to have a barcode reader than can simultaneously output to two different output devices, two data output tasks are required, instead of only one.

Details Text Image HTML KWIC

	U	Document I	Issue D	
3	<input type="checkbox"/>	US 5790536	199808	Hierarch
	<input type="checkbox"/>	A	04	Intelligen
4	<input type="checkbox"/>	US 5936224	199908	Method &
	<input type="checkbox"/>	A	10	symbols
				operator
5	<input type="checkbox"/>	US 5548108	199608	Method &
	<input type="checkbox"/>	A	20	
6	<input type="checkbox"/>	US 5914481	199906	Portable
	<input type="checkbox"/>	A	22	input are

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set 5 of 7 5,548,108

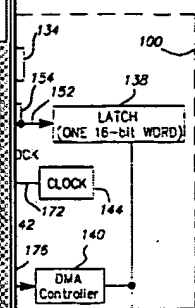
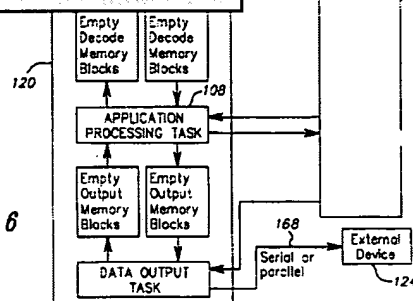
PROCESSOR  
MAIN  
MEMORY  
(RAM) 122

Fig. 6



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DERWENT-WEEK: 200251

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TITLE: Camera includes processor which gives high priority for  
execution of tasks controlled by switch operation

PATENT-ASSIGNEE: CANON KK[CANO]

PRIORITY-DATA: 2000JP-0319399 (October 19, 2000)

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
JP 2002131811 A	May 9, 2002	N/A	006	G03B 017/00

APPLICATION-DATA:

PUB-NO	APPL-DESCRIPTOR	APPL-NO	APPL-DATE
JP2002131811A	N/A	2000JP-0319399	October 19, 2000

(A) 01)特許出願公開番号  
特開2002-131811  
(P2002-131811A)  
(00)公開日 平成14年5月9日(2002.5.9)

5-72-11(参考)  
B 17/00 Q 3H030  
N 5/225 F 3H051  
B 17/11 N 5C022

主請求 従属請求 請求項の数 5 OL (全 5 項)

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代理人 1000097641

弁理士 岸田 立行 (外 3 名)

一ム(参考) 20020 M3D1

20051 A01 E025 E028 E032 E005

E040

50022 A017 A015 A017 A020 A022

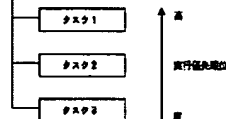
A032 A074

## (57)【要約】

【課題】リアルタイムOSによってプログラムの実行状態を制御するマイクロプロセッサ搭載のカメラにおける操作に対する応答性とプログラムの生産性を向上させる。

【解決手段】カメラのタスクとして、スイッチ操作による制御を行うタスク(タスク1)、フィルム給送タスク(タスク2)、画像読み取りを行うタスク(タスク3)の中で、実時間応答性の高い処理を行うタスクの実行優先度を、実時間応答性の低い処理を行うタスクの実行優先度よりも高く、すなわち、タスク1の優先度を最も高く、次いでタスク2、タスク3を最も低い優先度とした。

## タスクの優先度



	U	Document	Issue D	
3	<input type="checkbox"/>	US 4864511 A	198909 05	Automat
4	<input type="checkbox"/>	JP 2002131811 09 A	200205 09	Camera for execu
5	<input type="checkbox"/>	US 5913062 A	199906 15	Conferer local and providing
6	<input type="checkbox"/>	US 2002009182	200207 11	Intermed a central

### Detailed Description Text - DETX (43):

In step 310, the CPU 14 selects one of the contours determined under steps 302-308, and determines an orientation of the symbol image within the stored image. Under step 310, the CPU 14 can employ some of the same techniques employed under step 114. For example, the CPU 14 can select the first contour to be fully identified under one of the steps 302-308. Alternatively, the CPU can select the contour produced by the highest priority task in the finding set of modules 301. Based on the selected contour, the CPU 14 determines an orientation of the symbol image within the stored image by performing various techniques, such as those described in the patents and applications listed above with respect to the set of finding modules 301.

Current US Original Classification - CCOR (1):

235/462.1

Details Text Image HTML KWIC

	U	Document	Issue D	
2	<input type="checkbox"/>	US 5895906 A	199904 20	Hand-he module a
3	<input type="checkbox"/>	US 5790536 A	199808 04	Hierarch intelligen
4	<input type="checkbox"/>	US 5936224 A	199908 10	Method symbols operator
5	<input type="checkbox"/>	US 5548108 A	199608 20	Method a

Details Text Image HTML

Details Text Image HTML Full

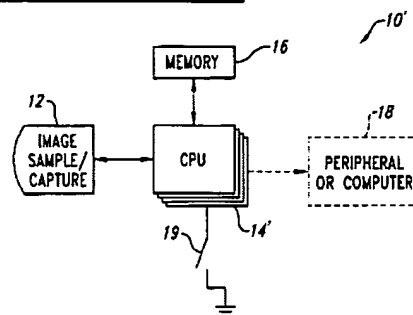


Fig. 2

## Detailed Description Text - DETX (23):

The channel side control processor 323, also known as channel processor, is a complete microprocessor that controls all activity on the channel side of the TCU 111. In a presently preferred embodiment of the invention, it consists of a high power, 16-bit microprocessor chip, with associated EPROM and RAM memories, clocks, interrupt handlers, registers, and parity generators and checkers. As such, the channel processor 323 is a multi-tasking, interrupt-driven processor. It responds immediately to tasks with a high priority than the task it is processing and stores a program address in memory, so that it can return to the previous job where it left off.

## Detailed Description Text - DETX (96):

Having described the LMU 106 in some detail, the following will explain the requirements for interfaces within the LSM 108, the LMU 106, its associated software, and operating procedures. As explained herein above, the REI 156 is the communications path between the LCU 109 and the electronics which are

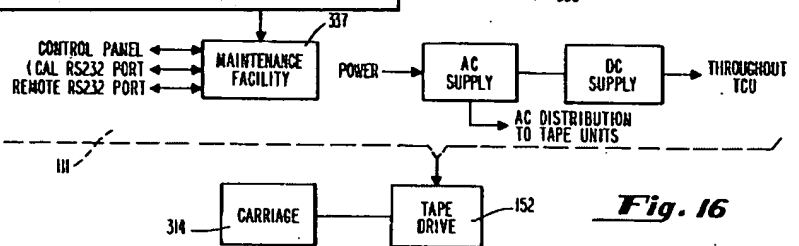
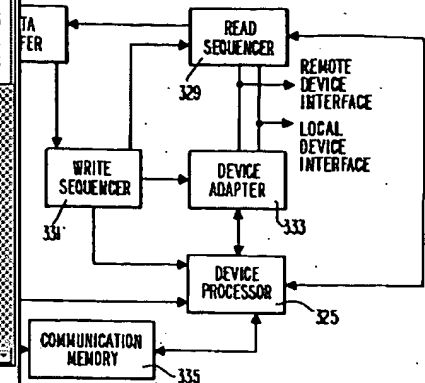


Fig. 16

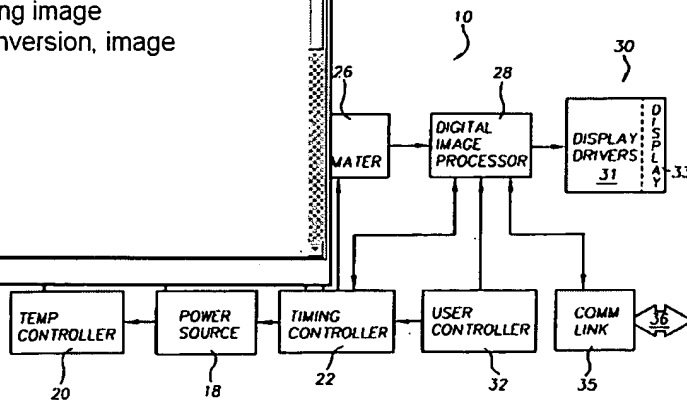
	U	Document	Issue D
1	A	US 4932826 199006	Automat 12
2	A	US 4928245 199005	Automat 22
3	A	US 4864511 198909	Automat 05
4	JP	2002131811 200205	Camera for exect 09

# Official Notice

KWIC

## Detailed Description Text - DETX (112):

Referring back to FIG. 1, the timing controller 22 provides overall timing control of the A/D, the analog signal processor, and the CCD imager to synchronize image acquisition and signal processing. One example timing controller in accordance with the invention consists of a programmable logic device that embodies a control state machine for synchronizing image integration, image signal readout, analog processing, A/D conversion, image frame sequence formatting, and digital image processing.



U.S. Patent

Dec. 3, 2002

Sheet 1 of 22

US 6,489,992 B2

	U	Document	Issue D	
13	<input type="checkbox"/>	US 6473062 B1	200210 29	Intelliger
14	<input type="checkbox"/>	US 6489992 B2	200212 03	Large fie
15	<input type="checkbox"/>	US 2001001936 1 A1	200109 06	Low-light
16	<input type="checkbox"/>	US 5880777 A	199903 09	Low-light

## Detailed Description Text - DETX (30).

Elements 125, 130, 132, 133, 134, 136, 138, 140 of FIG. 10 are substantially similar to corresponding elements shown in FIG. 9. However, exposure-dependent look-up table 142 is added downstream of the intersection of neighborhood processing block 132 and the R, G and B components of the images.

Exposure-dependent look-up table 142 includes a first look-up table (LUT1) which operates on the long-exposure image. A typical function implemented by LUT1 is  $LUT1(I)=5 * I.\sup.0.6$ . Likewise, exposure-dependent look-up table 142 includes a second look-up table (LUT2) which operates on the short-exposure image. A typical function implemented by LUT2 is  $LUT(I)=I.\sup.1.1$ . The use of the exposure-dependent look-up table 142 thereby enhances the dynamic range (histogram) of the bright area, thus improving the contrast and compensating for the loss of the saturation of the color in the bright areas which is due to the addition of background DC level from the long exposure frame. Moreover, LUT1 and LUT2 can be modified so as to include the gain factor, thereby allowing the three by three convolution kernel of neighborhood processing block 132 to be simplified to include a central element of epsilon (.epsilon.) and eight peripheral elements of negative one eighth (-1/8).

US 5247366 A  
 Patent Number: 5,247,366  
 Date of Patent: Sep. 21, 1993

719,320 1/1988 Als ..... 750,930  
 5,247,366 5/1990 Nagasaki et al ..... 756,443  
 5,247,366 5/1990 Gerson et al ..... 759,209

## OTHER PUBLICATIONS

See, "Image Processing in the Context of a Visual Model", Proceedings of the IEEE, 60(7), Jul. 1972, pp. 841-842.

See, "Towards the Unification of Three Visual and Two Visual Models in Brightness Perception", IEEE Trans Systems, Man Cybernetics 19(3), Apr. 1989, pp. 370-382.

See, Digital Imaging Processing, Second Edition, Wiley, pp. 185-186.

See, Zernike, John K. Peng  
 An Agent of Flow—William H. Clippert, Ronald W.

## ABSTRACT

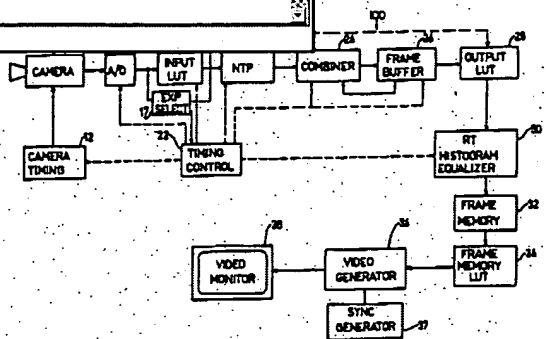
Apparatus is a color wide dynamic range video system which takes a plurality of images at different exposure levels, applies neighborhood processing to the images, and then combines the components of the images.

23 Claims, 10 Drawing Sheets

Details | Text | Image | HTML | KWIC

	U	Document	Issue D	
1		US 5247366 199309	Color wid	
	A	21		
2		US 5767993 199806	Holograp	
	A	16		
3		US 2002003913 200204	Methods	
	A1	04	control	
4		US 5124913 199206	Rule-bas	
	A	23	final scal	

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## Detail Description Paragraph - DETX (14):

[0024] DSC systems may be even more versatile with the ability to annotate images with text/speech. The preferred embodiment programmable DSP allows easy inclusion of a modem and/or a TCP/IP interface for direct connection to the Internet. DSCs may run complex multi-tasking operating systems to schedule the various real-time tasks.

## Detail Description Paragraph - DETX (18):

[0028] (1) Preview mode has data flow as illustrated in FIG. 2. ARM 130 sets CCD 150 into high-frame-rate readout mode (reduced vertical resolution). ARM 130 enables preview engine 104 and sets the appropriate registers for the default parameters. The raw CCD data is streamed into preview engine 104 and, after preview engine processing, is streamed into SDRAM 160. ARM 130 enables TV encoder 106 to display the preview engine output. Preview engine 104 processing (hardware) includes gain control, white balance, CFA interpolation, down-sampling, gamma correction, and RGB to YUV conversion. ARM 130 commands DSP 122 to perform auto exposure and auto white balance whenever required. DSP

122 processing includes auto exposure, auto white balance, and auto focus. ARM



US 20020041761A1

(a) Pub. No.: US 2002/0041761 A1

(a) Pub. Date: Apr. 11, 2002

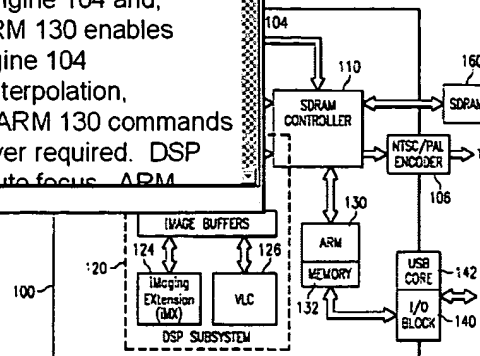
of provisional application No. 60/215,000, filed on Jan. 29, 2000. Non-provisional of provisional application No. 60/218,415, filed on Feb. 14, 2000. Non-provisional of provisional application No. 60/255,484, filed on Dec. 28, 2000.

## Publication Classification

Int. Cl.<sup>7</sup> G03B 17/48  
U.S. Cl. 396/429

## ABSTRACT

This Still Camera (DSC) includes separate preview and burst mode compression/decompression engines, a pipeline, CCD plus CCD controller, and memory plus memory controller. ARM microprocessor and DSP share control. Color filter array interpolation by use of green sub-frequency added to red and blue plus interpolation.



	U	Document	Issue D	
15	<input type="checkbox"/>	US 6438594 B1	20020820	Deliverin interface
16	<input type="checkbox"/>	US 2002013568 3 A1	20020926	Digital st
17	<input type="checkbox"/>	US 2002004176 1 A1	20020411	Digital st
18	<input type="checkbox"/>	US 2002002760	20020307	Digital st

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Detail Description Paragraph - DETX (14):

[0047] DSC systems may be even more versatile with the ability to annotate images with text/speech. The preferred embodiment programmable DSP allows easy inclusion of a modem and/or a TCP/IP interface for direct connection to the Internet. DSCs may run complex multi-tasking operating systems to schedule the various real-time tasks.

Detail Description Paragraph - DETX (19):

[0052] (1) Preview mode has data flow as illustrated in FIG. 2. ARM 130 sets CCD 150 into high-frame-rate readout mode (reduced vertical resolution). ARM 130 enables preview engine 104 and sets the appropriate registers for the default parameters. The raw CCD data is streamed into preview engine 104 and, after preview engine processing, is streamed into SDRAM 160. ARM 130 enables TV encoder 106 to display the preview engine output. Preview engine 104 processing (hardware) includes gain control, white balance, CFA interpolation, down-sampling, gamma correction, and RGB to YUV conversion. ARM 130 commands DSP 122 to perform auto exposure and auto white balance whenever required. DSP

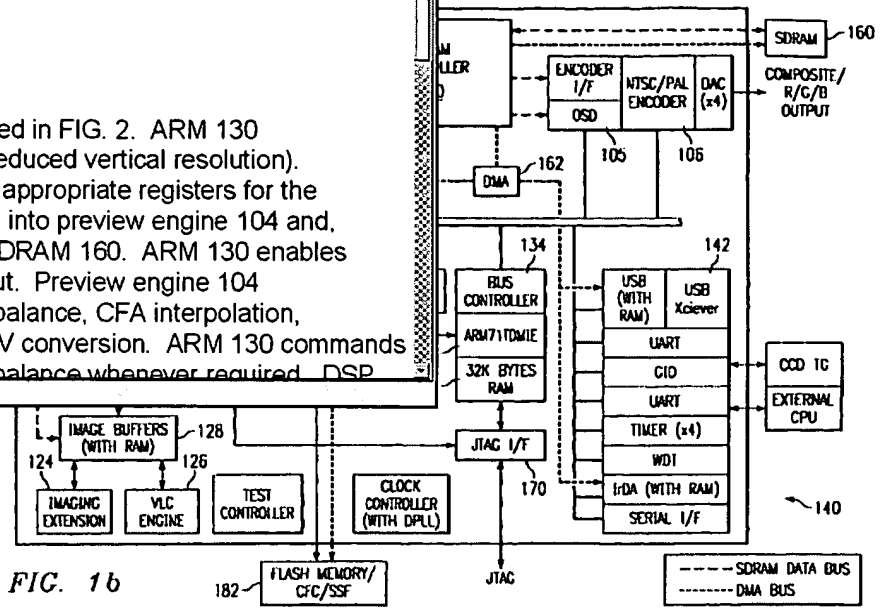


FIG. 16

	U	Document I	Issue D	
19		US 2002001544 7 A1	200202 07	Digital st
20		US 2002001239 8 A1	200201 31	Digital st
21		US 2002001205 5 A1	200201 31	Digital st
22		US 2002001205 31	200201 31	Digital st

## Detail Description Paragraph - DETX (14):

[0046] DSC systems may be even more versatile with the ability to annotate images with text/speech. The preferred embodiment programmable DSP allows easy inclusion of a modem and/or a TCP/IP interface for direct connection to the Internet. DSCs may run complex multi-tasking operating systems to schedule the various real-time tasks.

## Detail Description Paragraph - DETX (19):

[0051] (1) Preview mode has data flow as illustrated in FIG. 2. ARM 130 sets CCD 150 into high-frame-rate readout mode (reduced vertical resolution). ARM 130 enables preview engine 104 and sets the appropriate registers for the default parameters. The raw CCD data is streamed into preview engine 104 and, after preview engine processing, is streamed into SDRAM 160. ARM 130 enables TV encoder 106 to display the preview engine output. Preview engine 104 processing (hardware) includes gain control, white balance, CFA interpolation, down-sampling, gamma correction, and RGB to YUV conversion. ARM 130 commands DSP 122 to perform auto exposure and auto white balance whenever required. DSP 122 processing includes auto exposure, auto white balance, and auto focus. ARM

US 20020135683A1

(10) Pub. No.: US 2002/0135683 A1  
(43) Pub. Date: Sep. 26, 2002

## Related U.S. Application Data

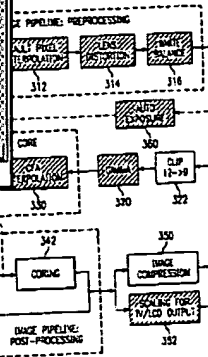
Provisional application No. 60/172,763, filed on Dec. 20, 1999. Provisional application No. 60/176,272, filed on Jan. 14, 2000. Provisional application No. 60/177,432, filed on Jan. 21, 2000. Provisional application No. 60/214,951, filed on Jan. 29, 2000. Provisional application No. 60/215,000, filed on Jan. 29, 2000.

## Publication Classification

Int. Cl.<sup>7</sup> H04N 5/235, H04N 5/231  
U.S. Cl. 348/222; 348/262; 348/223;  
348/346

## ABSTRACT

Pre-scaling is a digital image with pixel intensities and by a linear combination of pixel intensities and relative intensity distribution values.



	U	Document	Issue D	
14	<input type="checkbox"/>	US 5946667 A	199908 31	Data pro instrume
15	<input type="checkbox"/>	US 6438594 B1	200208 20	Deliverin interface
16	<input type="checkbox"/>	US 20020135683 A1	200209 26	Digital st
17	<input type="checkbox"/>	US 2002004176	200204 11	Digital st

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Full

FIG. 16 shows the relative DC signal (called "gain") as a function of the scanning exposure  $\eta$  and the ratio  $k$  of spot size  $\sigma_y$  to raster pitch  $p$ . The plateau in FIG. 16 represents the region of operating parameters wherein the phosphor is fully discharged. Thus, according to the first aspect of the present invention operating parameters are employed that insure operation on this plateau. As seen from FIG. 16, the exposure required to saturate the gain decreases as the spot size increases, for a given raster pitch. However, as spot size is increased, frequency response decreases. FIG. 17 shows the product of the gain and the slow-scan MTF at a fixed frequency  $\nu_y$ , for a circularly symmetric gaussian beam. From FIG. 17 it is seen that as  $k$  ( $\sigma_y/p$ ) is increased for a given exposure, the gain-MTF product (contrast transfer function CTF) at first increases because of the increase in gain. Then the product decreases because of the loss in spatial resolution. Thus, there is an optimal ratio  $k$  (in the sense of maximizing the system CTF) in the range of 0.2 to 0.3 depending upon the scan exposure  $\eta$ . Thus, according to a preferred mode of practicing the present invention, for a raster scanned read out with a gaussian shaped beam, the value of  $k$  ( $\sigma_y/p$ ) is between 0.2 and 0.3.

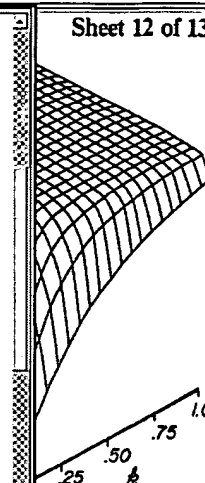


FIG. 16

	U	Document I	Issue D	
1	<input type="checkbox"/>	US 4762998 A	198808 09	Method of transparen
2	<input type="checkbox"/>	US 2002003913 A1	200204 04	Methods

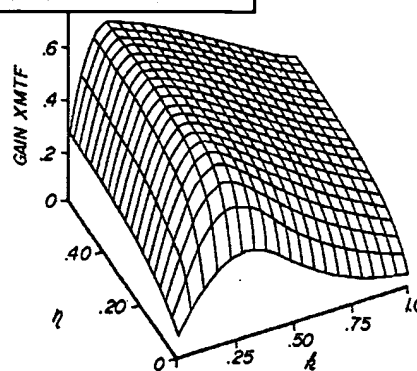


FIG. 17

embodiments. However, in the fourth embodiment, the radiological image is acquired on a low-contrast but wide-latitude mammographic film 600. This embodiment and the third embodiment differ in the source of the digitized image 40. The acquisition system, in this example, uses a relatively inexpensive conventional mammographic intensifying screen cassette 620. The cost ratio between this screen cassette 620 and a typical current digital mammographic system can be several orders of magnitude, e.g., approximately 1000 times. The standard screen-film acquisition and exposure technique and the conventional mammographic x-ray system (not shown here) will be unchanged for use in this embodiment. The high voltage of the x-ray generator typically is in the range of 25 to 35 KVP (kilovolt peak) or, as discussed below, can be raised to a level in the 40 to 55 KVP range. By reducing the average contrast gradient  $G$  of the mammographic film 600 say from about 3.0 to about 2.0, or to 1.5 or even less, we pick up substantial gain in exposure latitude.



US 20020054697A1

(19) Pub. No.: US 2002/0054697 A1

(43) Pub. Date: May 9, 2002

and which is a continuation-in-part of application No. 08/438,432, filed on May 10, 1995, now patented, which is a continuation-in-part of application No. 08/129,233, filed on Sep. 23, 1993, now abandoned.

## Publication Classification

Int. Cl.<sup>7</sup> G06K 9/00  
U.S. Cl. 382/128

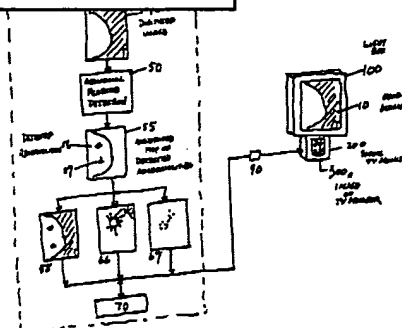
## ABSTRACT

x-ray system acquires an initial low-contrast, wide latitude ( $G=1.5$ , or  $G=2$  or less) x-ray image of a breast. A sensing system automatically finds suspected abnormalities in the breast by processing the low contrast initial image, then automatically converts the initial x-ray image to a narrower, narrow latitude image at the location of the detected abnormalities to thereby facilitate diagnosis and treatment. The technology includes effective ways to store, process and display the various images, and can be used to other types of images.

Details Text Image HTML KWIC

U	Document I	Issue D	
3	US 5049916	199109	Automati
	A	17	paramete
			extra sys
4	US 5792601	199808	Composi
	A	11	preparati
5	US 20020054697 A1	200205	Compute
6	US 2001003368	200110	Compute

Details Text Image HTML

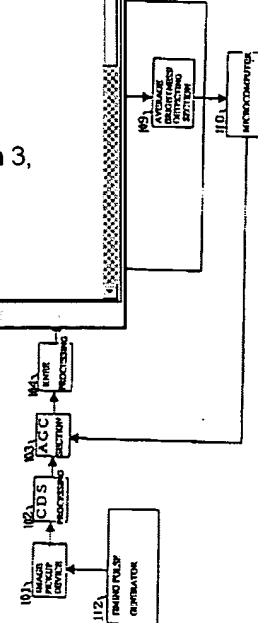


Details Text Image HTML Full

## Detail Description Paragraph - DETX (37).

[0048] A gradation correcting section 8 corrects the gradation of the mixed signal in such a manner that contrast of the gradation is emphasized when the histogram frequency of an image is large. A main signal processing signal 11 receives a gradation corrected signal produced from the gradation correcting section 8. An average brightness detecting section 9 detects an average brightness value based on the mixed signal. The microcomputer 10 inputs the average brightness value detected by the average brightness detecting section 9. The microcomputer 10 compares the detected average brightness value with a predetermined target brightness value. When the detected average brightness value is lower than the target brightness value, the microcomputer controls the AGC section 3 to increase the gain for the long-term exposure signal, thereby increasing the level of a video signal. On the other hand, when the detected average brightness value is higher than the target brightness value, the microcomputer controls the AGC section 3 to decrease the gain of AGC section 3, thereby decreasing the level of a video signal. In this manner, to control the level of a video signal, the microcomputer calculates an optimum gain to be set in the AGC section 3 and controls the gain of the AGC section 3 to the calculated value.

Sheet 3 of 4 US 2001/0008419 A1



Details Text Image HTML KWIC

	U	Document	Issue D	
3		US 2002003913 7 A1	200204 04	Methods control
4		US 5124913 A	199206 23	Rule-bas final scat
5		US 2001000841 9 A1	200107 19	Solid sta

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the signal synchronously at the pixel rate 25. The digital signal that is representative of the detected intensity of the light that is imaged from the illuminated object is applied to a digital signal processor (DSP), micro-controller or microprocessor that usually processes the images acquired, hereinafter referred to as processor 52. Processor 52 has the necessary memory resources, I/O and computing capabilities to handle the interface and algorithms described herein. The digitizing performed by ADC 50 and the processing performed by processor 52 can be deported to separate calibration or processing equipment, if the system does not require standalone calibration or sophisticated processing. The processor 52 controls all of the calibration steps as described herein. The values of the corrected intensity matrix 46 are calculated in processor 52. These values are then converted per FIG. 14 and loaded in the programmable light source sequencer 56. The light source sequencer is a logic device that has: either ISP (In Situ Programming) capability, such as a CPLD (Complex Programmable Logic Device), or FPGA (Field Programmable Gate Array) using Flash, E.sup.2 or RAM based technology, or any equivalent capability that allows full programming of a individual pulse width control on many outputs,



10) Patent No.: **US 6,473,062 B1**  
 40) Date of Patent: **Oct. 29, 2002**

4,981,817 A 1/1991 Dolnik et al.  
 5,315,182 A 8/1994 Brown et al.  
 5,335,782 A 1/1995 Bhargava et al. .... 235-435  
 5,602,410 A 5/1997 Brown  
 6,327,489 B1 12/2001 Bhargava et al. ... 2509-41.1

and by examiner

Attorney: Stephen—High Starch  
 Name: Examiner—Narciso E. Kovachik  
 (Attorney, Agent, or Firm—Mentel & Gendel; Wayne  
 Kelly)

#### ABSTRACT

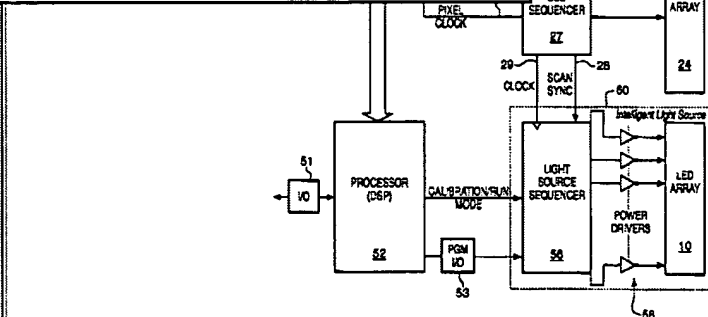
shown is a intelligent light source that is capable of  
 lighting a uniform illumination image across the surface of  
 illuminated object analyzed by an optical detector. This is  
 accomplished by individually controlling each lighting  
 element of a linear array of light elements. Cal-  
 ibration of the array is accomplished by sequentially illu-  
 minating each optical element of the source and building up  
 a matrix of normalized detected data. The matrix is then  
 read and multiplied by a linear array of ones to generate  
 calibration data. The calibration data are then used to  
 program a simple logic device that allows accurate digital  
 control of the intensity of each individual light element.

5 Claims, 11 Drawing Sheets

Details | Text | Image | HTML | KWC

	U	Document I	Issue D	
11	<input type="checkbox"/>	US 6371672 B1	200204 16	Imager for interface customiz
12	<input type="checkbox"/>	US 2003014465 O A1	200307 31	Integrate photoabl
13	<input type="checkbox"/>	US 6473062 B1	200210 29	Intelligen
14	<input type="checkbox"/>	US 6489992 B2	200212 03	Large fie

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## Detailed Description Text - DETX (52):

In one embodiment, the flash memory 1112 includes a direct memory access. The customized rasterizer board 312 may also be a high density board having multiple tracing layers for providing a modularized imager design. The customized programmable logic device (CPLD) 1108 formats data for the one or more pen driver boards 1200 (FIG. 9), and provides a data pathway between the microprocessor 1106 and the one or more pen driver boards 1200 (FIG. 9).

Embodiments are also envisioned in which the customized programmable logic device (CPLD) 1108 is also used as a high speed device for quickly processing the imaging data, and converting it into a bitmap. The customized programmable logic device (CPLD) 1108 is specifically design to process information 1000 times faster than if a microprocessor-based architecture were used.

Embodiments are also envisioned wherein the customized programmable logic device (CPLD) 1108 may also include either a programmable logic array (PLA), a programmable array logic (PAL), a field-programmable gate array (FPGA), a programmable logic device (PLD), or a combination thereof, to provide similar processing speeds.

11 of 18

US 6,371,672 B1

sterizer Printed Circuit Board)

	U	Document	Issue D	
9		JP 2002290787 A	200210 04	IMAGE F
10		US 5802203 A	199809 01	Image se
11		US 6371672 B1	200204 16	Imager f interface customiz
12		US 2003014465	200307 31	Integrate photoabl

FIG. 6B

## ABSTRACT:

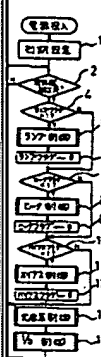
**PURPOSE:** To improve the function of a controller, and to reduce its cost by integrating an exposure scan control unit of a copying machine, an AC system control unit, and a main input/output control function, to one controller.

**CONSTITUTION:** An I/O control circuit 30 is integrally constituted of an exposure scan control unit, an AC system control unit and a main input/output control function. In this way, a circuit board 30 executes i) a positioning control for executing the constant-speed control of a scanner driving servomotor 58 of a variable exposure scanning system and the position control of a mirror driving motor 56, ii) an AC system control for executing the light quantity control of an exposing lamp 61, the temperature control of fixing heaters 62, 63 and the ON/OFF control of a main driving motor 64, iii) a developing bias voltage control, and iv) an I/O control except a copying sequence which is executed by a system control circuit 10, etc. In this way, by providing the circuit 30 for processing in parallel the management of an input/output data to other sequence than the copying sequence, by a multi-task, the arrangement and racking of a wire harness are simplified, the assembling work is executed efficiently, and the cost can be reduced.

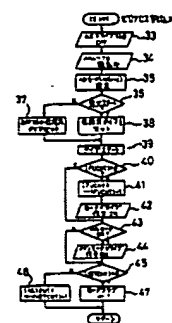
COPYRIGHT: (C)1988,JPO&Japio

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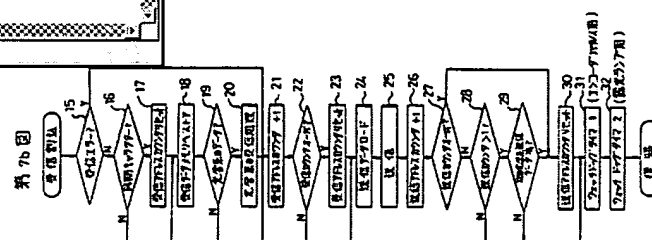
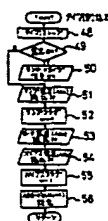
第 7a 図



第 7c 図



第 7d 図



	U	1	Document ID	Issue Date	
10			US 20040042829 A1	20040304	Compact by belt
11			JP 63101867 A	19880506	CONTROL
12			US 6160982 A	20001212	Copy she



**TITLE:** Electronic camera having a communication function

- KWIC

[0050] FIG. 5 is a flow chart of procedures used by the electronic still camera of the embodiment of the present invention. In this flow chart, for the convenience of explanation, both flow of the photography mode and the communication mode are described. However, for normal control by a microprocessor, a multitask OS (Operating System) method, for example, is generally adopted. In that case, the tasks for the photography mode and the tasks for controlling communication, etc., can be executed in parallel.

Publication Mar. 18, 2004 Sheet 9 of 13 US 2004/0051785 A1

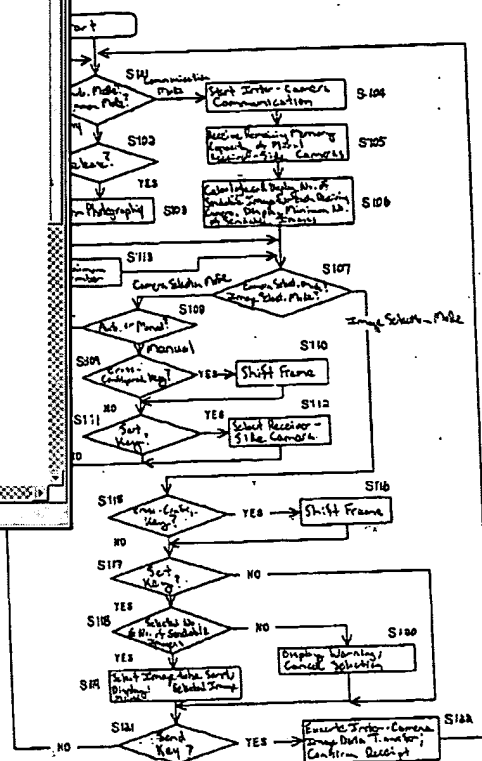


FIG. 11

	U	1	Document ID	Issue Date	
2			EP 424803 A	19910502	Digitally c holding di text inform
3			US 20040051785 A1	20040318	Electronic
4			US 5133024 A	19920721	Image da

by the CCD sensor. This procedure always carries out the same cycle beginning with the voltage 0 and ending with the voltage  $U_{max}$ . The waiting time after the application of a zero voltage to the piezoelectric enables the latter to become stabilized. The waiting time before the start of the acquisition avoids the acquisition of a frame which may have been exposed before the application of the desired exposure conditions. The end of the exposure of an image is indicated on the acquisition cards by the start of the transfer of the corresponding image. The use of an exposure time shorter than the image transfer time prevents the image from being affected by transient states. Giving the process maximum priority prevents the disturbance of acquisition by other system tasks under a multitask operating system. The six images are acquired successively and in real time (no image lost) by the acquisition card in order to minimize the time during which vibrations can affect the result. Each image has the horizontal dimension of  $h_{pix}$  and vertical dimension of  $v_{pix}$ . During acquisition, images are transferred automatically by the acquisition card into an array which is reserved for them in the computer's central memory. Following the acquisition procedure, there is a resulting array  $I[a,b,i,j]$ , the index  $a$  corresponding to the phase difference, the index  $b$  corresponding to the image (phase-shifted or not phase-shifted), the indices  $i$  and  $j$  being the coordinates in pixels and varying respectively from 0 to  $h_{pix}-1$  and from 0 to  $v_{pix}-1$ .

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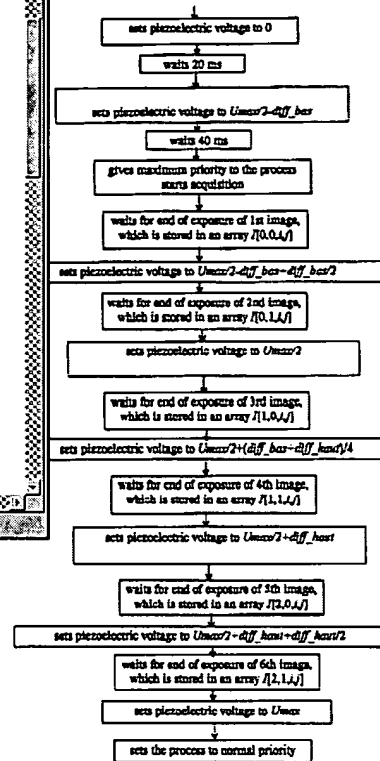


Fig. 11

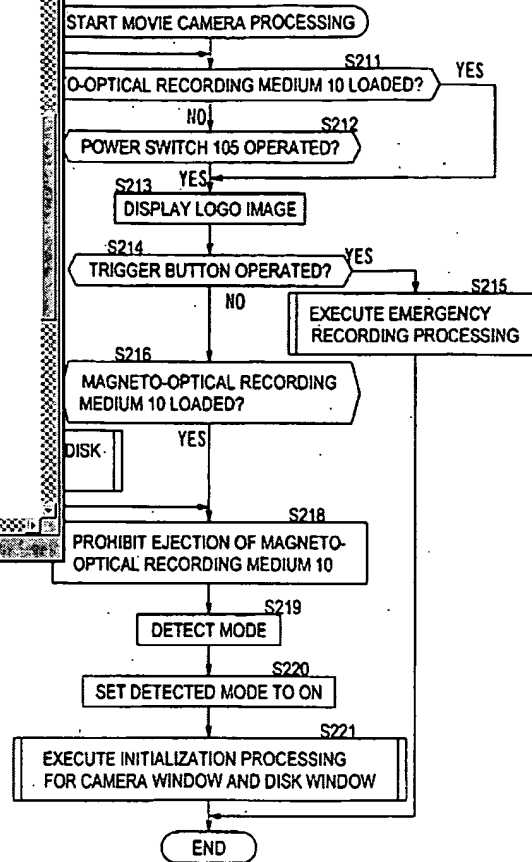
	U		Document ID	Issue Date	
28			US 20020039137 A1	20020404	Methods
29			US 6525875 B1	20030225	Microscopical object analysis
30			US 6185399 B1	20010206	Multicolor charge coupled device

to be output to an A/D conversion unit 22. The A/D conversion unit 22 converts the image signal provided by the image-capturing element 21, which is an analog signal, to a digital signal. The signal processing unit 23 implements exposure control of the image-capturing element 21 (e.g., aperture or auto-gain control), and also executes processing such as white balance correction, gamma correction and the like on the image signal provided by the A/D conversion unit 22 to be output to a frame memory 24.

#### Detail Description Paragraph - DETX (153):

[0259] Next, the camera window or disk window initialization processing implemented in step S221 in FIG. 27 is explained. It is to be noted that the camera window initialization processing and the disk window initialization processing can be executed simultaneously through multitasking. FIG. 35 is a flowchart illustrating the initialization processing for the camera window. First, in step S51, a decision is made as to whether or not the photographing mode is set to ON, and if it is decided that the photographing mode is not set to ON, the operation proceeds to step S252 in which the control unit 34 implements control on the display image generating unit 33 to display the camera icon 51 before ending the processing.

FIG.27



	U	Document ID	Issue Date	
30		US 6549949 B1	20030415	Fixed for environm
31		US 20030210898 A1	20031113	Image red dynamic i apparatus methods program
32		US 6434568 B1	20020813	Information

apparatus 40 includes an incubator enclosure 42, which has mounted on it an enclosure 44 for the imaging system, a shelf 46 adapted for supporting holders which are to be inserted into the incubator enclosure, an enclosure 48 for an input mechanism 50 (seen in FIG. 8) for introducing holders on the shelf 46 into the incubator enclosure 42, and a hopper 52 for receiving holders that have been ejected from the incubator enclosure. An alternative input means, not illustrated, includes a cartridge capable of containing a plurality of holders in a stack. Such a cartridge may be attached or fitted to the input mechanism in order to transfer holders from the cartridge into the incubator enclosure. A microprocessor 53 is connected to the mechanisms within the incubator enclosure 42. With multi-tasking, the microprocessor can provide several control functions, serving as a control means for the mechanisms which move and queue the holders within the incubator enclosure, as a way of controlling the timing of the taking of images by the camera, and as the counting means. The above referenced U.S. patent application Ser. No. 08/061,678, METHOD FOR THE EARLY DETECTION OF COLONY GROWTH, now U.S. Pat. No. 5,510,246, describes programming suitable for detecting and enumerating microbial colonies; the programming required to control the holder positioning means and the timing of the taking of video images depends on the user interface desired and on the exact physical arrangements and sizing of components, but the expedients required are well known to those of ordinary skill in the programming art.

Patent (19)

 (11) Patent Number: 5,744,322  
 (45) Date of Patent: Apr. 28, 1998

 PURSUANT TO AND IMAGING  
 DISPOSABLE  
 A CLIPPING DEVICE  
 USA

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 L. Mach, Shorewood, Scott D.  
 Cottage Grove, Thomas A.  
 PMA, Inc. of Minn.  
 a Mining and  
 Mining Company, St. Paul.

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 2 227 346 7/1990 United Kingdom 006M 1102  
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 "Electronic Colony Counter" by YSMF (3 pages) no date  
 provided.

## Application Data

Ser. No. 156,681, Dec. 17, 1993.

 C12Q 1/66; C12M 1/54  
 G06F 3/00; G06F 3/02; G06F 3/04;  
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 G06F 15/42; G06F 15/44; G06F 15/46;  
 G06F 15/48; G06F 15/50; G06F 15/52;  
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 G06F 15/66; G06F 15/68; G06F 15/70;  
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 G06F 15/78; G06F 15/80; G06F 15/82;  
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 G06F 15/90; G06F 15/92; G06F 15/94;  
 G06F 15/96; G06F 15/98; G06F 16/00;  
 G06F 16/02; G06F 16/04; G06F 16/06;  
 G06F 16/08; G06F 16/10; G06F 16/12;  
 G06F 16/14; G06F 16/16; G06F 16/18;  
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 G06F 19/38; G06F 19/40; G06F 19/42;  
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 G06F 19/80; G06F 19/82; G06F 19/84;  
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 G06F 19/92; G06F 19/94; G06F 19/96;  
 G06F 19/98; G06F 20/00; G06F 20/02;  
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 G06F 20/70; G06F 20/72; G06F 20/74;  
 G06F 20/76; G06F 20/78; G06F 20/80;  
 G06F 20/82; G06F 20/84; G06F 20/86;  
 G06F 20/88; G06F 20/90; G06F 20/92;  
 G06F 20/94; G

## Abstract Text - ABTX (1):

A hand-held processing system wherein a peripheral module may receive therein a computer processor basic module of standardized construction, with a user-immune real-time multi-tasking operating system. Advantageously the peripheral module or computer processor module may include a touch screen or other highly versatile and compact data input/output device adaptable to graphical and/or other input/output modes suitable for different applications, languages and the like.

## Brief Summary Text - BSTX (7):

In a preferred embodiment the standardized computer processor module is provided with a multi-tasking operating system such that battery monitoring software and diagnostic routines will run at a fixed priority level at all times while a wide range of applications software can be run concurrently without jeopardizing the reliability of the system under extended portable operating conditions. ■

## Brief Summary Text - BSTX (11):

The computer processor module may be employed with peripheral devices such as printers, laser bar code readers, RF modules, smart card interface modules,

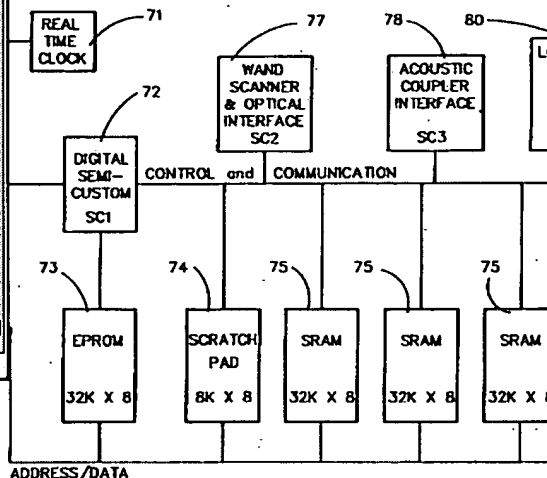


FIG. 4

	U	Document ID	Issue Dat	Tit
26	□	US 5679948 A	1997102	Constant luminescence source mo
27	□	US 5644728 A	1997070	Control systems
28	□	US 5227614 A	1993071	Core computer processor module assembled to form a pocket size d
29	□	US 5483049 A	1996010	Coupon exchanging and check wri

presently commercially available, and the decoding software in these devices can be adapted to the requirements of the PCMCIA defined PC card and ported to the particular circuitry used on the PC card. The details of the commercially available wand based barcode reading software is hereby incorporated by reference.

#### Detailed Description Text - DETX (135):

In the embodiment of FIG. 26, the adapter chip receives an interrupt from the decoder chip 538 via line 573 each time a character has been decoded and is ready for pickup. The adapter chip 536 then picks up the character and generates an IRQ interrupt to the host on line 574. A program 519 stored on the host computer controls operations of a microprocessor 516 in the host 500 to execute an interrupt service routine to retrieve the character from the adapter chip and place it in the keyboard buffer of the host. An exemplary program to perform the function of program block 519 is included herewith at Appendix A. This program is written in C++ and can be ported to any host with a suitable compiler. Alternatively, the program 519 could transmit the character to another application running on a multitasking host computer. In alternative embodiments, the program 519 can control the microprocessor to move the decoded character or message from the adapter chip 536 into the memory space shared between the PC card and the host.

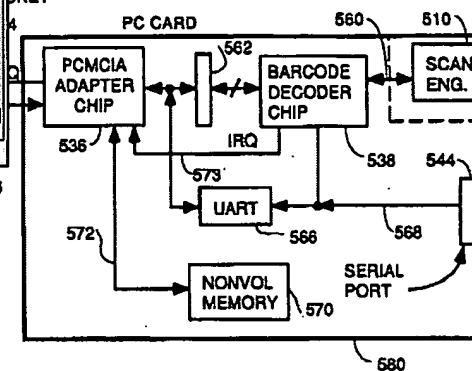
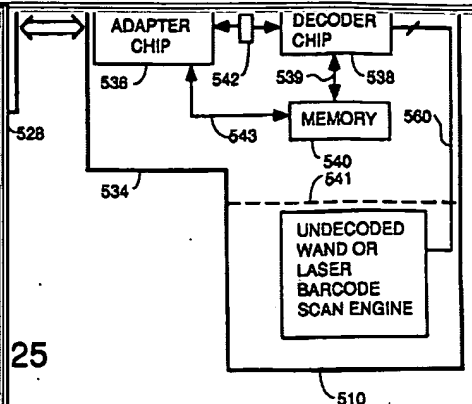


FIG. 26

	U	1	Document ID	Issue Date	
14			US 5845150 A	19981201	Modular c redundan source d
15			US 5671374 A	19970923	PCMCIA scanning computer
16			US 6536670 B1	20030325	PCMCIA barcode s

## Summary of Invention Paragraph - BSTX (9):

[0008] A desired imaging device would incorporate a single main processor that would be capable of running the operating system and application program as well as executing the capture and decode program for the image data. An imaging device that has a single processor capable of all of these operations provides a more streamlined and efficient apparatus, and may also use less expensive components. By eliminating from the overall imaging device architecture the need to incorporate a second processor and, in most instances, an associated PCB, the end-user will typically benefit from being provided a device that costs less, is more reliable and less complex. Thus, the invention teaches how to combine the heretofore separate and independent operations mandating multiple microprocessors, memories and transfer interfaces into a single processor capable of multiple operations. Such a combination is not merely the natural consequence of improvements in microprocessor capacity and capabilities because of the necessity to combine separate hardware, software and protocols into a single processor design. The invention teaches how to accomplish all of these disparate tasks with a central processor, and do so in a multi-tasking environment that was not present when using the prior art technique of employing a dedicated (single task) processor to execute the image capture and decode functions.

tes

Application Publication (10) Pub. No.: US 2002/0039457 A1  
(45) Pub. Date: Apr. 4, 2002

APPARATUS FOR IMAGE  
RECORDING IN A  
PROCESSING UNIT

(51) U.S. Cl. 382/305

(57) ABSTRACT

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6/17/2001

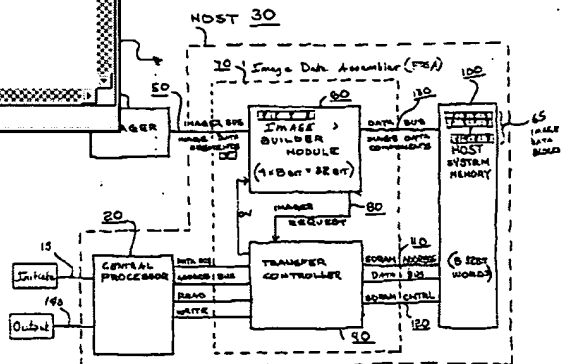
Application Data

provisional application No.  
Sep. 29, 2000.

a Classification

G06K 9/54; G06K 9/60

An improved method and device for capturing image data benefits from having a single central processor execute the operating system, and the image capture, decode and processing programs. A method for capturing of image data comprises transmitting image data from an image, assembling the image data, assigning a memory address to the assembled image data and transferring the assembled image data into system memory. This method is capable of central processing whereby the capturing of image data is executed via the main processor without having to involve a dedicated processor or incorporate external components, such as additional PCBs, external digital signal processing or external data storage. Additionally, an imaging device comprises an image builder module that receives image data from the image bus and assembles the data, and a transfer controller that initiates the image builder module and controls the transfer of image data into and out of memory.



	U	1	Document ID	Issue Date	
12			US 5761529 A	19980602	Method for having pl... identificat...
13			US 20020039457 A1	20020404	Methods centralize...
14			US 5845150 A	19981201	Modular c... redundan...

US-PAT-NO: 5048623

DOCUMENT-IDENTIFIER: US 5048623 A

TITLE: Combination weighing apparatus

KWIC

## Detailed Description Text - DETX (10):

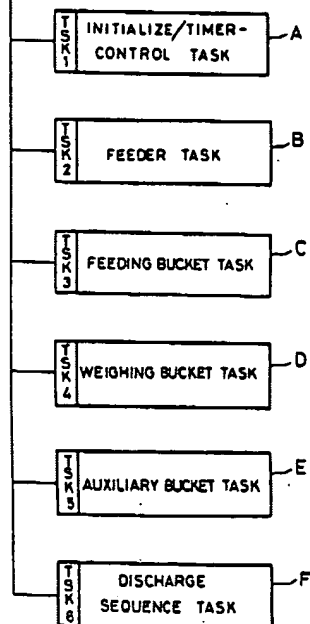
The ROM 42B of the microcomputer stores a Real-time Multi-task Operating System which is shown in FIG. 5 and comprises an initialize/timer-control task "TSK1", a feeder task "TSK2", a feeding bucket task "TSK3", a weighing bucket task "TSK4", an auxiliary bucket task "TSK5" and a discharge sequence task "TSK6", respectively labeled "A", "B", "C", "D", "E" and "F" in FIG. 5.

Sep. 17, 1991

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5,048,623

FIG. 5

Real-time Multi-task  
Operating System

	U	1	Document ID	Issue Date	
8			US 4590583 A	19860520	Coin tele
9			US 5048623 A	19910917	Combina
10			US 4868757 A	19890919	Computer



FIG. 1. Digital dictation system having a central station that includes component cards for interfacing to dictation stations and transcription stations and for processing and storing digitized dictation segments

— KWIC —

#### Detailed Description Text - DETX (29):

In the preferred embodiment of the present invention, the AT card 40 (FIG. 1) is a controller or a personal computer, well known to those skilled in the art, that is dedicated to running the modular digital dictation system 10 of the present invention. In the preferred embodiment, the AT card 40 is an IBM AT personal computer, specifically including a 80486 microprocessor running the OS/2 operating system. However, other microprocessors or operating systems well known to those skilled in the art may be used. The OS/2 operating system program is a multitasking system, broadly meaning that it can support many application programs running at the same time.

#### Detailed Description Text - DETX (135):

Other functions are performed at step 138 (FIG. 12), including creating the

Sep. 22, 1998

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5,812,882

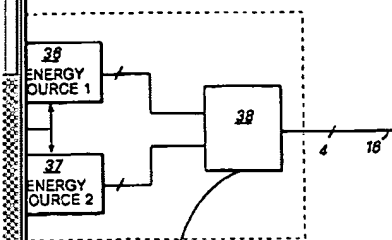


FIG. 4

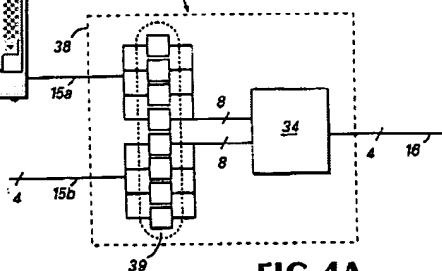


FIG. 4A

	U	1	Document ID	Issue Date	
3			US 6396497 B1	20020528	Computer
4			US 5812882 A	19980922	Digital dictation component, transcript dictation
5			US 6353436 B1	20020305	Graphical